Appendix B

Hitachi Releases 16-Bit Microcontroller with On-Chip Large Flash Memory

— Suitable for control of storage devices such as CD-R/RW and DVD-ROM/RAM, and incorporating large 512- Kbyte on-chip flash memory for shorter development time —

Tokyo, August 2, 2001— Hitachi, Ltd. (TSE: 6501) today announced the H8/3069F F-ZTAT™ microcontroller*, with large 512-Kbyte flash memory and 16-Kbyte RAM on-chip, as an addition to the H8/300H Series lineup of 16-bit microcontrollers. Sample shipments will begin in November 2001 in Japan.

With its large-capacity on-chip flash memory and RAM, the H8/3069F is suitable for control of storage devices such as CD-R/RW, DVD-ROM/RAM, and combined CD-RW and DVD-ROM/RAM devices. The provision of on-chip flash memory also allows program modifications to be carried out on-board, enabling system development time to be shortened.

Featuring a high-performance 16-bit H8/300H CPU core and a rich set of peripheral functions that include 16-bit timers, an A/D converter, DMA controller, and serial interface, and offering a comprehensive lineup that includes F-ZTAT versions with on-chip flash memory that enables shorter development times to be achieved, the H8/300H Series is widely used in the communication, information, OA, and industrial fields. Among such applications, the use of storage devices such as CD-R/RW, DVD-ROM/RAM, and HDDs as devices for handling large-volume multimedia data, including still and moving images, has experienced rapid growth in recent years.

Hitachi has previously released the H8/3062F, H8/3064F, and H8/3068F, with on-chip flash memory capacities of 128, 256, and 384 Kbytes, respectively, as F-ZTAT products for storage device control. But the increasingly sophisticated functionality of application products, including the advent of combined CD-RW and DVD-ROM/RAM devices, means ever larger program sizes, and at the same time there is a demand for large-capacity on-chip flash memory to enable extended system development times to be cut.

The H8/3069F has been developed to meet these market needs, offering the following features around a H8/300H CPU core.

[Product Features]

(1) Largest on-chip memory capacity in H8/300H Series
512 Kbytes of single-power-supply flash memory and 16 Kbytes of RAM are provided on-chip, allowing storage of a large system program. In addition, the flash memory programming speed is approximately three times faster than current products, offering a shorter write time despite the larger capacity.

(2) Enhanced flash memory programming method

Flash memory programming methods now inlcude the industry's first user boot mode in addition to the conventional boot mode and user programming mode. Previously, the boot program run when the device is powered on has only operated in a boot mode that initiates a fixed program that cannot be modified by the user, but in user boot mode, a user-written program can be run. This makes it possible to run a program written to meet specific user needs after powering on, such as selection of the interface to be used, or erasure of the flash memory.

In addition, the flash memory program/erase control program is built in as firmware, enabling programming/erasing to be executed simply by calling this program from the user program. This eliminates the previous need for a user-written control program, enabling the application device's system program to be simplified and development time to be shortened.

(3) High-speed operation, with a 25 MHz operating frequency at a power supply voltage of 5 V or 3.3 V

Logic circuits such as the CPU core run at a low voltage of approximately 1.9 V. An on-chip step-down circuit generates a voltage of approximately 1.9 V from a 5 V or 3.3 V external power supply voltage, making it possible to select the power supply voltage according to the voltage of the interface used, and to achieve high-speed operation with a minimum instruction execution time of 80 nanoseconds at the maximum operating frequency of 25 MHz on either power supply voltage.

On-chip peripheral functions include functions suited to storage device control such as three 16-bit timer channels, four 8-bit timer channels, eight high-precision 10-bit A/D converter channels, four DMA controller channels, and three serial interface channels.

The following software and hardware products are available to provide a development environment for the H8/300H Series:

- Software: C compiler, assembler, linkage editor, simulator/debugger
- Hardware: E6000 realtime emulator

The H8/3069F is available in a 100-pin plastic 0.5 mm pin pitch QFP or TQFP package. Use of the thin TQFP makes it possible to create slimmer systems.

Future plans include further extension of the product lineup with the development of higher-speed models and mask ROM models.

Note: * F-ZTAT (Flexible Zero Turn-Around Time) is a trademark of Hitachi, Ltd. F-ZTAT microcontroller is with on-chip flash memory and can be easy rewritten for program and system adjustment data.

< Typical Applications >

- Storage devices: CD-R/RW devices, DVD-ROM/RAM devices, combined CD-RW and DVD-ROM/RAM devices, HDD devices, etc.

< Prices in Japan > (For Reference)

Product Code		Package	Sample Unit Price (Yen)
H8/3069F	HD64F3069F	QFP-100	1,400
	HD64F3069TE	TQFP-100	1,500

< Specifications >

Item		Specification
Model Name		H8/3069F
CPU core		H8/300H
Operating frequency/power supply voltage		25MHz / 3.0 V to 3.6 V 25MHz / 4.5 V to 5.5 V
ROM		512-Kbyte flash memory Programming methods (3 kinds) • Boot mode • User programming mode • User boot mode
RAM		16 Kbytes
Address space		16 Mbytes
External data bus width		16/8 bits
Bus type		Non-multiplexed
DMA controller		4 channels
16-bit timer		3 channels
8-bit timer		4 channels
Watchdog timer		1 channel
Programmable timing pattern controller		16-bit output
SCI (synchronous/asynchronous)		3 channels
10-bit A/D converter	Inputs	8 channels
	External trigger function	Yes
8-bit D/A converter outputs		2 channels
External interrupts		7 channels
I/O ports		79
CS outputs		8
Packages		QFP-100 (14 mm × 14 mm, 0.5 mm pin pitch) TQFP-100 (14 mm × 14 mm, 0.5 mm pin pitch)

Appendix C

Consumer IC Advances -> MIPS, software make for smooth DVD decoding

EETIMES

MIPS, software make for smooth DVD decoding

By Alson Kemp, Senior Field Applications Engineer, Cirrus Logic, Fremont, Calif., EE Times
December 18, 2001 (1:12 p.m. EST)
URL: **http://www.eetimes.com/story/OEG20011218S0049**

Digital videodisk playback is a complicated process that requires decoding many different complex data types and coordinating the flow of time-sensitive data through a complex series of transformations. One of the major functions of a DVD player is the playback of compressed audio and video from the DVD disk. Using complex graphics, the menu display allows users to navigate the disk and select playback options and system configurations. Dramatic price decreases in VLSI silicon have created room for innovation for this rising consumer star, with cost-effective chips incorporating the large, complicated functional blocks required for DVD playback.

At the heart of a DVD player is the multifunction DVD chip. This block typically incorporates functions such as an MPEG-2 video decompressor, a DSP, a 32-bit microprocessor, I/O for audio, infrared for control and a built-in TV encoder or digital video output for a TV encoder. The processor may be a 32-bit RISC device with performance of approximately 100 Mips with separate instruction and data caches. Some microprocessors may have a memory-management unit, but some DVD chips have removed the MMU to reduce cost. Most microprocessors include integer multipliers and some, including the Cirrus/CS98100, include a multiply-accumulate unit to speed complex math operations.

The DVD loader includes the laser, pickup and servos. The loader also has a DVD controller to drive the servos and spindle, read data from the optics and present a suitable data interface to the DVD chip. Although there is no rule defining which loader interface a particular DVD player will use, market segments favor certain interfaces: Higher-end, multispeed or PC-focused loaders use an ATAPI/IDE interface; lower-end, single/double-speed or consumer-focused loaders use proprietary serial or 8-bit interfaces to reduce cost. DVDs have 2,048 byte sectors and like CDs, are encoded at a constant linear velocity, so that as the pickup's radius on t he disk is increased, the drive's spindle slows down.

Several I/O and memory buses are used. Typically, SDRAM is used as a data and program store for the processor, DSP and other functional blocks. Flash is used to store program and persistent data. Simple serial interfaces, such as the Sony/Philips digital interface, ports and UARTs, along with a port to provide infrared remote control functionality are included. Complex direct memory access hardware assists the CPU in moving blocks of data both around the chip and between external memory and devices.

Some DVD video packets are encrypted with the Content Scrambling System. DVD chips incorporate a CSS decryption block to offload decryption processing from the microprocessor. The video processor off-loads common graphics chores from the microprocessor. De-interlacing duties for progressive-scan systems, video scaling, frame-rate conversion, video mixing and zoom are all handled by the video processor. Subpictures, a custom DVD graphics format that is used for overlays, subtitles, menu highlighting and screen text, and on-screen display graphics are decoded by separate hardware modules and blended with the video processor output.

By using a combination of perceptual, predictive and entropy-encoding algorithms, MPEG compresses video by approximately 95 percent. Decompressing the resulting video is very compute-intensive, and so most DVD chips incorporate hardware MPEG video decoding. Although the decoder must only support a subset of MPEG-2's Main Profile @ Main Level (specifically geared to television resolutions and frequencies), most MPEG video decoders support many more resolutions and frequencies than the MPEG-2 standard specifies.

Most MPEG video decoders, for example, will decode MPEG video from video CDs and supervideo encoders and convert CCIR-601 or -656 digital video from the DVD chip's video output into analog signals for a television. The digital video data is presented to the encoder as 8-bit data, but many video encoders oversample and interpolate the data to 10 bit for improved video quality before converting it into composite, S-video or component video signals. The encoder must support Macrovision copy protection for DVD compliance. Progressive-scan video outputs are not yet common among mid- to low-end DVD players, but some DVD chips, such as the CS98100, support progressive-scan video capabilities.

All DVD players must have analog audio outputs, either stereo or 5.1 channel digital audio outputs, S/PDIF and standard optical TOSLINK . Some multichannel audio D/As are specifically tailored for the consumer DVD market and others are tailored for the high-end DVD player markets. The digital audio outputs are encoded using IEC 60958 for uncompressed pulse-code-modulated audio or IEC 61937 for AC3, Digital Theater Sound (DTS) or otherwise compressed audio.

An embedded real-time operating system runs on the microprocessor to provide basic functionality for a range of functions including booting, memory management, I/O, task cont rol, messaging, semaphores, timers, peripheral drivers and communications stacks. Support for the DVD and CD file systems, generally UDF and ISO9660, respectively, must also be provided by the operating system. A real-time operating system is necessary because of the time constraints imposed by the need to quickly respond to requests from the various functional blocks.

The microprocessor also handles demultiplexing audio, video and subpicture data. Each DVD packet/sector can contain a variety of data types that must be pulled apart and passed to specific decoders. Each sector can also carry a time stamp for synching audio and video. Audio and video decompression are handled by separate decoders, but decompressed streams must be presented to the user according to the data's time stamp.

Compressed audio on a DVD is stored as MPEG-2, Dolby Digital (AC-3) or DTS. Some DVD players can decode other audio formats such as MPEG-1 Layer 3, WMA and AAC. All of those encoding methods are perceptual coders and g ive compression ratios of around 5 to 10:1. The coders use knowledge of human auditory perception to remove sounds below the ear's threshold (a very soft 80-Hz tone), frequency-masked sounds (a 1-kHz tone might mask a 1.1-kHz tone that is 40 dB down), channel-masked sounds (a loud sound from the center channel can mask a soft sound in another channel), and temporally masked sounds (a quiet sound that follows a loud sound). Also, unused bandwidth from one channel can be allocated to a busier audio channel. The resulting bit stream is then entropy-

encoded to further reduce the bandwidth.

Because the software is specific to the chip and to a single application (the DVD player), the DVD chip vendor will often develop much of the required software and license it to the DVD system maker. The system maker can then tailor and brand the software to meet specific player needs. The DSP software is also responsible for post-processing of the audio. This post-processing can include effects such as pitch shifting for karaoke, the virtualization of stereo to multichannel, loudness, equalization and bass management.

Today's large DVD manufacturers use proprietary virtualization algorithms or preferred equalization algorithms, so the DSP must be programmable and the DVD chip vendor must either provide tools for OEMs to develop DSP software or in-house programmers to adapt software to the OEM's needs.

See related chart

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